IN THE CLAIMS

1. (Currently Amended) A synchronous integrated circuit device ~~having an output bus for outputting a plurality of output signals~~, comprising:

a clock input buffer configured to receive a system clock signal and to generate a buffered clock signal;

a delay line coupled to the clock input buffer, the delay line configured to receive the buffered clock signal and to generate a delayed clock signal; and

an output circuit coupled to the delay line, the output circuit including a plurality of output signal paths configured to output the plurality of output signals synchronously with the system clock signal by using the delayed clock signal;

wherein at least one of the output signal paths includes a delay circuit and an output buffer coupled to the delay circuit, each delay circuit is connected to a delay control circuit which determines the amount of delay required for the at least one of the output signal paths based upon feedback from the plurality of output signal paths, and each delay circuit is configured to provide a programmable delay to the delayed clock signal to generate a unique delayed clock signal which is used for clocking an output signal into the respective output buffer.

2. (Original) The device of claim 1, wherein the programmable delay provided by each delay circuit is programmed to decrease output skew across the output signals.

3. (Original) The device of claim 1, wherein the clock input buffer provides a first delay, each output signal path provides a second delay, and the delay line provides a third delay based upon a delay model of the sum of the first delay and the second delay.

4. (Original) The device of claim 1, further comprising a phase detector to control the delay line based upon a phase difference between the buffered clock signal and a signal generated by applying a delay model to the delayed clock signal.

5. (Original) The device of claim 1, wherein the programmable delay provided by each delay circuit is programmed dynamically.

6. (Original) The device of claim 1, wherein the programmable delay provided by each delay circuit is programmed statically.

7. (Original) The device of claim 1, wherein the programmable delay provided by each delay circuit is programmed based upon output skew during operation of the device.

8. (Original) The device of claim 1, wherein the programmable delay provided by each delay circuit is programmed based upon an output skew between a first output signal that was output from the respective output signal path and a second output signal.

9. (Original) The device of claim 1, wherein the device has an initialization mode of operation wherein the output signals are toggled, and the programmable delay provided by each delay circuit is programmed during initialization operation.

10. (Currently Amended) A synchronous integrated circuit device ~~having an output bus for outputting a plurality of output signals~~, comprising:

a clock input buffer configured to receive a system clock signal and to generate a buffered clock signal;

a delay locked loop (DLL) coupled to the clock input buffer and configured to receive the buffered clock signal and to generate a delayed clock signal; ~~and~~

an output circuit coupled to the DLL, the output circuit including a plurality of output signal paths configured to output the plurality of output signals synchronously with the system clock signal by using the delayed clock signal;

wherein at least one of the output signal paths includes a delay circuit and an output buffer coupled to the delay circuit, each delay circuit configured to provide a programmable delay to the delayed clock signal to generate a unique delayed clock signal which is used for clocking an output signal into the respective output buffer; and

wherein the programmable delay is set based upon feedback from others of the output signal paths to synchronize the output signal with other output signals.

11. (Original) The device of claim 10, wherein the programmable delay provided by each delay circuit is programmed to decrease output skew across the output signals.

12. (Original) The device of claim 10, wherein the clock input buffer provides a first delay, each output signal path provides a second delay, and the DLL provides a third delay based upon a delay model of the sum of the first delay and the second delay.

13. (Original) The device of claim 10, wherein the DLL includes a delay line coupled between the clock input buffer and the output circuit, and a phase detector to control the delay line based upon a phase difference between the buffered clock signal and a DLL clock signal generated by applying a delay model to the delayed clock signal.

14. (Original) The device of claim 13, wherein the DLL also includes a clock driver circuit coupled between the delay line and output circuit, the clock driver circuit configured to drive the delayed clock signal to each of the plurality of output signal paths.

15. (Original) The device of claim 10, wherein the DLL comprises a digital DLL.

16. (Original) The device of claim 10, wherein the DLL comprises an analog DLL.

17 (Currently Amended) A synchronous integrated circuit device ~~having an output bus for outputting a plurality of output signals~~, comprising:

a clock input buffer configured to receive a system clock signal and to generate a buffered clock signal;

a delay line coupled to the clock input buffer, the delay line configured to receive the buffered clock signal and to generate a delayed clock signal; ~~and~~

an output circuit coupled to the delay line, the output circuit including a plurality of output signal paths configured to output the plurality of output signals synchronously with the system clock signal by using the delayed clock signal;

wherein the output signal paths each includes a variable delay circuit and an output buffer coupled to the delay circuit, each delay circuit configured to provide an independent variable delay to the delayed clock signal to generate a unique delayed clock signal for clocking an output signal into the respective output buffer; and

wherein each of the variable delay of each of the delay circuit is programmed based upon the delay of others of the plurality of output signals from other output buffers.

18. (Original) The device of claim 17, wherein the variable delay provided by each of the delay circuits is determined so as to decrease output skew across the output signals.

19. (Original) The device of claim 17, wherein the clock input buffer provides a first delay, the output signal paths provide a second delay, and the delay line provides a third delay based upon a delay model of the sum of the first delay and the second delay.

20. (Original) The device of claim 17, further comprising a clock driver circuit coupled between the delay line and the output circuit, the clock driver circuit configured to drive the delayed clock signal to each of the plurality of output signal paths.

21. (Original) The device of claim 17, wherein the independent variable delay provided by each variable delay circuit is dynamically determined.

22. (Original) The device of claim 17, wherein the independent variable delay provided by each variable delay circuit is statically determined.

23. (Original) The device of claim 17, wherein the independent variable delay provided by each variable delay circuit is based upon output skew measured during operation.

24. (Original) The device of claim 17, wherein the independent variable delay provided by each variable delay circuit is based upon output skew between a first output signal that is output from the respective output signal path and a second output signal.

25. (Original) The device of claim 17, wherein the device has an initialization mode of operation wherein the output signals are toggled, and the independent variable delay provided by each delay circuit is programmed during initialization operation.

26. (Original) The device of claim 17, wherein one of the output signal paths is the slowest output signal path, and the variable delay provided by each of the delay circuits is individually programmed based upon the slowest output signal path so as to align the plurality of output signals, thereby decreasing skew across the output signals.

27. (Original) The device of claim 17, wherein one of the output signal paths is defined as a reference output signal path, the delay circuit for the reference output signal path provides a midpoint delay, and the delay circuits for the remaining output signal paths provide less or more than the midpoint delay if the corresponding output signal path is slower or faster than the reference output signal path, respectively.

28-42. (Canceled)

43. (Currently Amended) A method of outputting a plurality of output signals ~~on an output bus~~ of a synchronous integrated circuit device with decreased output skew, comprising:

receiving a system clock signal;

delaying the system clock signal to generate a delayed clock signal;

applying the delayed clock signal to a plurality of output signal paths;

in each of the output signal paths, using the delayed clock signal to output the plurality of output signals synchronously with the system clock signal; and

in at least one of the output signal paths, providing a programmable delay to the delayed clock signal to generate a unique delayed clock signal which is used for clocking an output signal

out from the respective output signal path by determining the programmable delay based upon delay of the plurality of output signals.

44. (Original) The method of claim 43, wherein each programmable delay is provided to decrease output skew across the output signals.

45. (Original) The method of claim 43, wherein receiving the system clock signal includes buffering the system clock signal.

46. (Original) The method of claim 43, wherein delaying the system clock signal includes detecting a phase difference between the system clock signal and a signal generated by applying a delay model to the delayed clock signal, and using the detected phase difference to control the amount of delay provided to the system clock signal.

47. (Original) The method of claim 43, wherein delaying the system clock signal includes applying the system clock signal as an input signal to a DLL.

48. (Original) The method of claim 43, wherein providing each programmable delay takes place dynamically.

49. (Original) The method of claim 43, wherein providing each programmable delay includes determining output skew during an initialization mode of device operation.

50. (Original) The method of claim 43, wherein applying the delayed clock signal to the plurality of output signal paths includes driving the delayed clock signal, thereby increasing fanout of the delayed clock signal.

51. (Currently Amended) A method of outputting a plurality of output signals on an output bus of a synchronous integrated circuit device with decreased output skew, comprising:

receiving a system clock signal;

delaying the system clock signal to generate a delayed clock signal;

applying the delayed clock signal to a plurality of output signal paths;

in each of the output signal paths, using the delayed clock signal to output the plurality of output signals synchronously with the system clock signal; ~~and~~

in each of the plurality of output signal paths, providing an independent variable delay to the delayed clock signal to generate a unique delayed clock signal for use in clocking an output signal out from the respective output signal path; and

determining the delay of each of the plurality of output signals to determine the independent variable delay for each of the plurality of output signal paths.

52. (Original) The method of claim 51, wherein each independent variable delay is provided to decrease output skew across the output signals.

53. (Original) The method of claim 51, further comprising determining the output signal path which is the slowest output signal path, wherein providing each variable delay is based upon the slowest output signal path so as to align the output signals.

54. (Original) The method of claim 51, further comprising defining one of the output signal paths as a reference output signal path, wherein providing the variable delay for the reference output signal path includes providing a midpoint delay, and providing the variable delay for the remaining output signal paths includes providing less or more than the midpoint delay if the corresponding output signal path is slower or faster than the reference output signal path, respectively.

55-67. (Canceled)

68. (Currently Amended) An apparatus for outputting an output signal on an output bus of a synchronous integrated circuit device with decreased output skew, comprising:

an input circuit for receiving a system clock signal;

a delay line coupled to the input circuit for delaying the system clock signal;

an output circuit coupled to the delay line for outputting an output signal, the output circuit including a programmable delay circuit for providing a programmable delay to the delayed system clock signal for use in clocking out the output signal; and

wherein the programmable delay is determined from the amount of delay of the output signals based upon feedback from s plurality of output signal .

69. (Currently Amended) An apparatus for outputting a plurality of output signals ~~on an output bus~~ of a synchronous integrated circuit device with decreased output skew, comprising:

an input circuit for receiving a system clock signal;

a delay line coupled to the input circuit for delaying the system clock signal;

an output circuit coupled to the delay line for outputting a plurality of data output signals, the output circuit including at least one programmable delay circuit for providing a programmable delay to the delayed system clock signal for use in clocking out at least one of the data output signals with decreased skew across the bus;

a feedback path is connected to the output circuit for receiving an amount of delay of the data output signals based; and

a delay control circuit connected to the feedback path and to the programmable delay circuit for determining the programmable delay based upon the delay of the data output signals .

70. (Canceled)

CONCLUSION

Applicant respectfully submits that the claims are in condition for allowance, and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney at (612) 373-6904 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

AARON M. SCHOENFELD ET AL.

By their Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. Box 2938
Minneapolis, MN 55402
(612) 373-6904

Date Oct 20, 2004 By Daniel J. Kluth
Daniel J. Kluth
Reg. No. 32,146

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 20 day of October, 2004.

Tina Kohout
Name

Signature